# PATENT ABSTRACTS OF JAPAN

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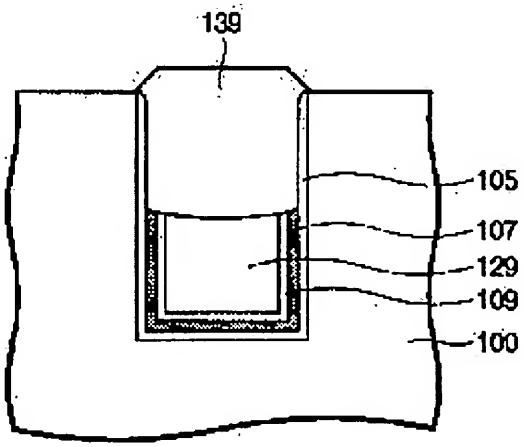
## (54) METHOD FOR FORMING TRENCH ELEMENT ISOLATION FILM

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a method for forming a trench element isolation film.

SOLUTION: The trench element isolation film according to the present invention comprises the steps of forming the trench by an etching after forming a trench etching pattern on a substrate, forming a silicon nitride film liner on an inner wall surface of the trench, exposing an upper portion of the trench liner by recessing a first filled oxidation film by a wet process, removing a top portion of the liner by an isotropic etching and filling a recessed space of the trench by a second filling oxidation film. The step of forming the trench etching pattern on the substrate substantially further includes depositing the silicon nitride film on the substrate on which a pad oxidation film is formed, patterning, and forming a thermal oxidation film on the inner wall surface by an annealing so as to repair etching damages between the step of forming the trench and the liner.

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* NOTICES *



1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

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DRAWINGS

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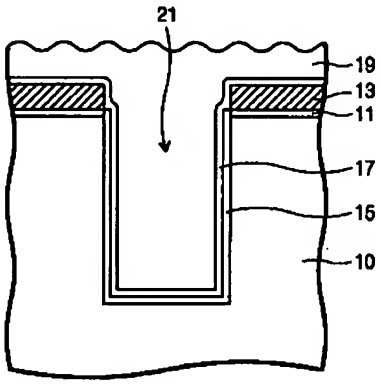
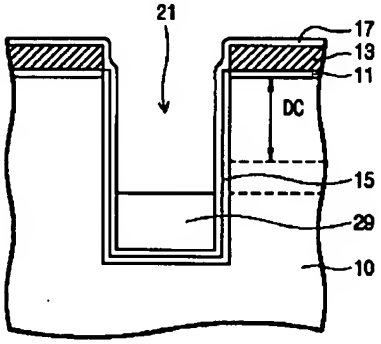
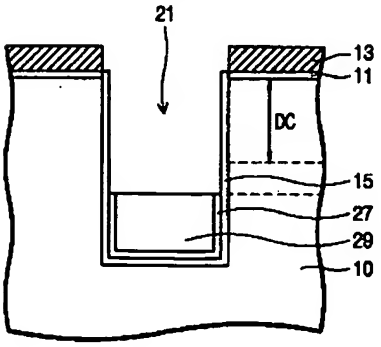
[Drawing 1]
(従来技術)



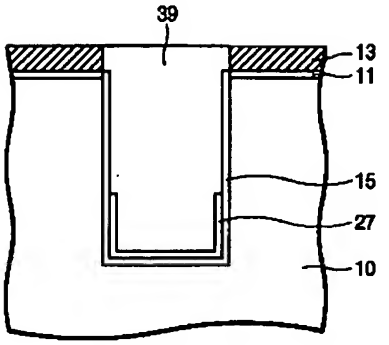

[Drawing 2]
(従来技術)



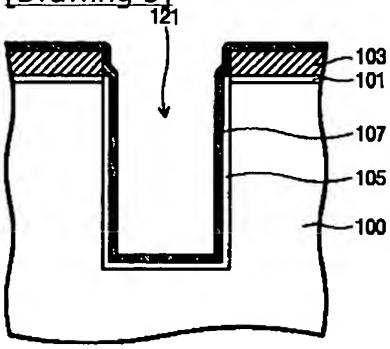

[Drawing 3]
(従来技術)



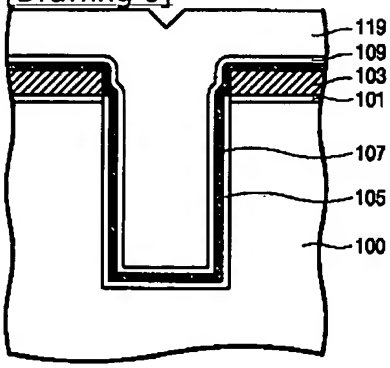
[Drawing 4]
(従来技術)



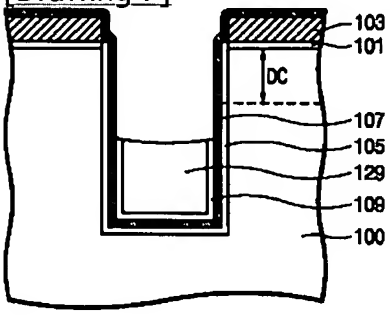

[Drawing 5]



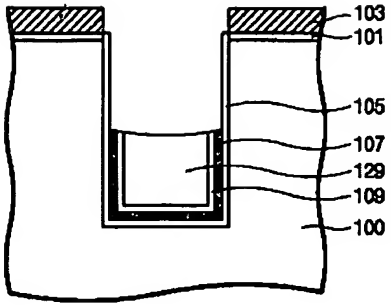

[Drawing 6]



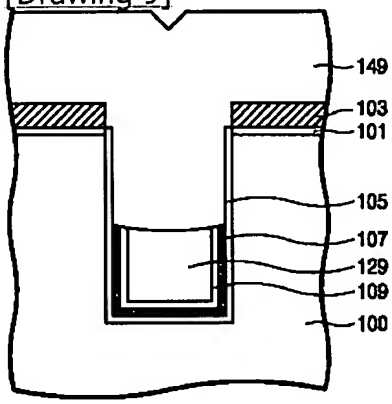

[Drawing 7]



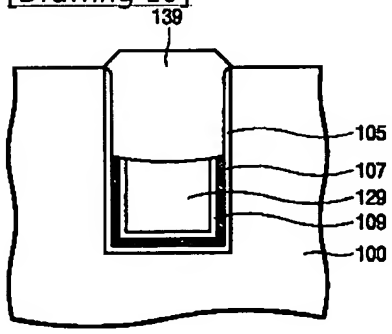

[Drawing 8]




[Drawing 9]




[Drawing 10]

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## DETAILED DESCRIPTION

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[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention starts the formation approach of the trench component demarcation membrane of a semiconductor device, and relates to the formation approach of a trench component demarcation membrane of having the nitride liner from which the upper part was removed by the detail, more.
[0002]
[Description of the Prior Art] According to high integration of a component, the approach of filling up with an oxide film the trench formed in the substrate is used for the trench mold isolation approach developed in order to solve the limit by the BAZU beak (bird's beak) in LOCOS (local oxidation of silicon) mold isolation. Therefore, although there is no problem of a BAZU beak, there are problems, such as volume expansion by oxidation of consecutiveness of the substrate of the substrate, heat stress [ by the difference of the quality of the material of a demarcation membrane ], and demarcation membrane circumference. As one approach of solving such a problem, the silicon nitride liner was formed in the wall of a trench, and the approach of filling up with an oxide film was developed. A silicon nitride liner acts as barrier which prevents diffusion of oxygen, it prevents that the substrate of the trench circumference oxidizes like a consecutive heat process by this, and stress may be decreased.
[0003] In etching the upper part of a silicon nitride liner, and a dent (dent's) phenomenon's occurring, filling up with a polish recon layer the silicon nitride field removed by etching and forming the gate in the phase of removing the silicon nitride of the active field used as etching prevention film at the time of forming a trench when using a silicon nitride liner, there is a problem which the so-called "the hump (hump)" generates.
[0004] Moreover, since the property which catches an electron on a front face is the strong matter, a silicon nitride is a silicon nitride liner in the both sides of the channel of an MOS (metal oxide silicon) transistor, in case a carrier moves along with a channel especially by the thermal oxidation film and the silicon nitride interface, catches an electron and changes the substantial flow of a carrier. The depth of a channel is shallow, and when width of face is wide, such a problem does not have big effect relatively. However, in the case of the semiconductor device which carries out trench isolation according to high integration of a component, generally the width of face of a channel is narrow, and there are many parts which adjoined the silicon nitride of the both sides of a channel. Therefore, prehension of the electron of the silicon nitride used as a liner affects the movement magnitude (flow) of a carrier. When the source / drain current flows through a channel especially with a P channel transistor, when becoming a hole and catching an electron by the nitride of the both sides of a channel, the substantial flow of a hole increases and a hot carrier effect (hot carrier effect) generates the main carriers.
[0005] In order to prevent prehension of the electron of the silicon nitride liner of the both sides of a

channel, the approach only the substantial depth of a channel removes a silicon nitride liner is indicated by U.S. Pat. No. 5,940,717. This approach is explained with reference to drawing 1 - drawing 4 R> 4.

[0006] Reference of drawing 1 forms the trench etching pattern 13 in the substrate 10 with which the pad oxide film 11 was formed for a silicon nitride a laminating and by carrying out patterning. And the wall of a trench 21 is oxidized thermally, the thermal oxidation film 15 is formed, the laminating of the silicon nitride is further carried out to the whole surface thinly, and the trench wall liner 17 is formed. Then, the laminating of the photoresist film 19 is carried out by the spin coating approach, and it is filled up with a trench 21.

[0007] If drawing 2 is referred to, etchback of the photoresist film filled up with the trench 21 will be carried out, and the residual (recessed) photoresist film 29 by which the recess was carried out will be formed. Ashing (ashing) is mainly carried out in an oxygen plasma ambient atmosphere. A recess process is carried out until the residual photoresist film 29 remains in the location below effective depth DC of a channel with a trench 21.

[0008] Reference of drawing 3 removes the silicon nitride liner 17 exposed to the substrate 10 by etching. Usually, a silicon nitride liner is also removed by Fukashi from whom the liner exposed by dry type plasma etching was removed, and the photoresist was removed.

[0009] If drawing 4 is referred to, the photoresist which remained to the trench will be removed, the laminating of the CVD (chemical vapor deposition) oxide film will be carried out to the whole surface, and the trench component demarcation membrane 39 filled up with a trench will be formed. And trench etching pattern 13 front face which consists of a silicon nitride of an active field is exposed by flattening etching of CMP (chemical mechanical polishing) etc. The silicon nitride of an active field is removed by consecutive wet etching, and the trench component demarcation membrane 39 is formed completely.

[0010] However, when using such an approach, etching of the surrounding film is damaged according to the process which carries out the recess of the photoresist, and the process in which a silicon nitride liner is removed by etching of the upper part of a trench. If the silicon nitride of an active field is etched partially and the height of the whole substrate is not equal, the level of a component demarcation membrane becomes less fixed at the CMP process of the CVD oxide film carried out on the basis of the top face of this film etc. Moreover, when damage on etching on a trench side attachment wall occurs, there is a possibility that current leakage may occur with the component formed henceforth.

[0011]

[Problem(s) to be Solved by the Invention] This invention is for solving the trouble mentioned above, and aims at offering the formation approach of a trench component demarcation membrane that change of the component actuation by prehension of the electron of a silicon nitride liner is prevented with a trench component discrete-type semiconductor device, and a hot carrier effect can be prevented.

[0012] This invention fixes level of a component demarcation membrane while removing a silicon nitride liner partially, and sets it as other purposes to offer the formation approach of a trench component demarcation membrane that current leakage of a trench circumference component can be prevented.

[0013] This invention prevents the oxidization of the trench circumference by the silicon nitride liner, and sets it as other purposes to offer the formation approach of trench isolation without the trouble of a dent.

[0014]

[Means for Solving the Problem] The phase which this invention for attaining the above-mentioned purpose forms a trench etching pattern in a substrate, and forms a trench by etching, The phase which forms a silicon nitride liner in the wall of a trench, and the phase which fills up a trench with

the 1st reclamation oxide film, The phase of carrying out the recess of the 1st reclamation oxide film according to a wet process, and exposing the upper part of the liner of a trench, It is related with the formation approach of the trench component demarcation membrane of a semiconductor device including the phase where isotropic etching removes the upper part of a liner, and the phase which fills up with the 2nd reclamation oxide film the space where the recess of the trench was carried out.
[0015] The phase which forms a trench etching pattern in a substrate by this invention carries out the laminating of the silicon nitride to the substrate with which the pad oxide film was formed preferably, carries out patterning and is made. Moreover, it is desirable to include further the phase where the thermal oxidation film is formed of ANIINGU for restoring damage on etching to the wall of a trench between the phase which forms a trench, and the phase which forms a liner.
[0016] And in order to decrease the substrate film dependency of a reclamation oxide film and to raise philharmonic a gap between the phase which forms a liner, and the phase which fills up a trench with the 1st reclamation oxide film, it is desirable to carry out plasma surface treatment. However, since it is easy to damage a liner in this process, in order to protect a liner from plasma surface treatment, it is LP on a liner. It is desirable to contain between the phase which forms a liner for the phase which carries out the laminating of a buffer oxide film like the HTO (high temperature oxide) film by CVD (low pressure chemical vapor deposition), and the phase which fills up a trench with the 1st reclamation oxide film.
[0017] Since carrying out until the above-mentioned process which carries out a recess becomes low below at the predetermined channel depth in which the front face of the 1st reclamation oxide film became settled to the transistor component formed henceforth with the trench, although a recess is carried out by the wet process in this invention in order that the 1st reclamation oxide film may prevent the etching damage on surrounding has sufficient effectiveness to prevent prehension of the electron by the silicon nitride liner, it is desirable.
[0018] As for the phase where isotropic etching removes the upper part of a liner, in this invention, it is desirable that wet carries out with a phosphoric-acid solution.
[0019] This invention is the trench of a P channel field which prehension of the electron by the silicon nitride liner may make generate a hot carrier effect, and has especially effectiveness. Therefore, as for the trench by this invention, it is desirable to carry out only within the trench of a P channel transistor field.
[0020] Furthermore, as for the approach of this invention, it is desirable to include further the phase of carrying out CMP to the 2nd reclamation oxide film, and the removal phase over a trench etching pattern.
[0021] In this invention, the 1st reclamation oxide film and said 2nd reclamation oxide film are preferably formed by the CVD approach, and, as for at least one side, being formed by the SOG film is desirable among the 1st reclamation oxide film and the 2nd reclamation oxide film.
[0022] The phase of removing the upper part of a liner in this invention is HDP preferably. It carries out with the phase which fills up with said 2nd reclamation oxide film the space by which the recess was carried out by CVD.
[0023]
[Embodiment of the Invention] Hereafter, the desirable operation gestalt of this invention is explained to a detail with reference to attached drawing. In addition, in drawing, when it is that to which an interlayer exists among these even if directly located on the layer of others [ layer / the ] when a layer is shown are located on other layers or a substrate, or a substrate, both sides shall be meant.
[0024] If drawing 5 is referred to, by the thickness whose pad oxide film 101 is 100-200A, the laminating of the silicon nitride with a thickness of 500A will be carried out, it will carry out patterning at the silicon substrate 100 formed thinly, and the trench etching pattern 103 which a substrate exposes in a trench field will be formed. Patterning forms with photolithography the photoresist

pattern which is not illustrated, and is made by the approach of carrying out etching of as opposed to a silicon nitride for this with an etching mask. Furthermore, the laminating of the thin oxide film may be carried out on a silicon nitride (wall of a trench), and you may use by the hard surface mask blank to silicon nitride etching.

[0025] If the trench etching pattern 103 is formed, a substrate 100 will be etched into a depth of 2000-5000A by making this into an etching mask, and a trench 121 will be formed. And in order to restore the crystal damage generated at the etching process in the wall of a trench 121, the thermal oxidation film 105 is thinly formed by thermal oxidation. The silicon nitride liner 107 is formed in the substrate with which it was formed, the wall 105, i.e., the thermal oxidation film, of a trench 121, by CVD. It is the same process as the usual trench isolation approach which was mentioned above.

[0026] When drawing 6 is referred to, it is LP on the silicon nitride liner 107. By the CVD approach, the HTO oxide film 109 is thinly formed as a buffer oxide film. The laminating of this HTO oxide film 109 is carried out before the plasma treatment carried out in order to abolish a substrate film dependency on a substrate front face before formation of a reclamation oxide film, and it is a kind of a buffer oxide film. And a trench is filled up with the 1st reclamation oxide film 119. Under the present circumstances, the 1st reclamation oxide film 119 is the CVD approach, especially HDP. It is desirable to be formed by the CVD (high density plasma enhanced chemical vapor deposition) approach. Again Ozone TEOS USG (O3 tetra ethyl ortho silicate undoped silicate glass), A BPSG (boro phospho silicate glass) oxide film, the SOG film, etc. can use it for the 1st reclamation oxide film 119 with which the SOG film is filled up with a trench 121 preferably especially. The 1st reclamation oxide film cannot be completely filled up with the whole trench in this phase, either.

[0027] SOG film, such as polysilazane (polysilazane), may be formed as a reclamation oxide film as the aspect ratio of a trench increases.

[0028] If drawing 7 is referred to, the recess of the 1st reclamation oxide film 119 will be carried out according to a wet process, for example, whole surface wet etching, and the upper part of the liner of a trench will be exposed. If whole surface anisotropic etching is used at this time, since a trench side attachment wall will receive etching damage, wet etching is used. It is desirable to carry out until the phase which carries out the recess of the 1st reclamation oxide film 119 according to a wet process comes to below predetermined effective channel depth DC, i.e., the location where the front face (residual oxide film 129) of the 1st reclamation oxide film 119 is lower than effective channel depth DC, of components, such as a transistor by which the front face 129 of the 1st reclamation oxide film 119, i.e., a residual oxide film, is formed around a trench. Consequently, the silicon nitride liner 107 is exposed as the recess of the reclamation oxide film filled up with a trench was carried out.

[0029] As for at least one side, being formed by the SOG film is desirable among the 1st reclamation oxide film and the 2nd reclamation oxide film (explained in full detail below). This is because the upper part is removable by processing the SOG film before hardening with a suitable wet solution carrying out the recess of the SOG film also besides the usual wet etching, when using a reclamation oxide film by the SOG film. Hardening may be carried out to the SOG film from which the upper part was removed.

[0030] Reference of drawing 8 all removes a liner, in [ isotropic etching's having removed the exposed silicon nitride liner 107 (upper part of a liner) by wet / which contains a phosphoric-acid solution preferably /, namely, the residual oxide film 129 remaining it ]. Although dry type isotropic etching may be carried out instead of wet isotropic etching, when the laminating gestalt of a liner 107 and etching damage are taken into consideration, plasma etching or RIE (reactive ion etching) is not suitable, therefore its wet isotropic etching is desirable using wet isotropic etching, especially a phosphoric-acid solution.

[0031] Reference of drawing 9 fills up with the 2nd reclamation oxide film 149 the space where the laminating of the 2nd reclamation oxide film 149 was carried out on the substrate in the condition

that the liner was removed in the upper part of a trench, and the recess of the trench was carried out. Under the present circumstances, as for a trench, it is desirable to fully fill up with the 2nd reclamation oxide film 149. The approach and the quality of the material which were used for the above-mentioned 1st reclamation oxide film can use the 2nd reclamation oxide film similarly. as an approach -- the CVD approach -- especially -- desirable -- HDP the CVD approach -- desirable -- it can be used -- moreover, ozone TEOS Especially, it is desirable, the SOG film is desirable to the 2nd reclamation oxide film 149, and USG, BPSG, the SOG film, etc. can be used. And it is desirable to carry out the removal process of the trench etching pattern by whole surface anisotropic etching and/or the CMP process over the 2nd reclamation oxide film preferably on the basis of the top face of a trench etching pattern, and to carry out flattening of the 2nd reclamation oxide film.
[0032] Or it is HDP in the phase of drawing 9 without removing a liner separately in the phase of drawing 8 . The laminating (restoration) of the space by which the recess was carried out with the 2nd reclamation oxide film is carried out, and the upper part of a liner can be removed by CVD at it and coincidence. HDP In CVD, since etching is carried out by turns with a laminating, while a liner is removed, the laminating of the 2nd reclamation oxide film is also possible.
[0033] Drawing 10 shows an example of the trench component demarcation membrane formed of this invention, and shows the condition that wet etching removed the silicon nitride used by the trench etching pattern 103 of the condition of drawing 9 . Therefore, the thermal oxidation film 105 is formed in the substrate of the trench in the completed trench component demarcation membrane, the silicon nitride liner 107, the thin HTO oxide film 109, and the residual oxide film 129 of the 1st reclamation oxide film exist in the lower part at the inside, and the demarcation membrane 139 in which flattening of the 2nd reclamation oxide film was carried out, and it remained exists in the upper part. However, since the demarcation membrane 139 from the HTO oxide film 109, the residual oxide film 129 of the 1st reclamation oxide film, and the 2nd reclamation oxide film is all an oxide film, it can also be said that an oxide film fills up the lower part of the wall of the thermal oxidation film 105 of a trench with the remaining trench space where the silicon nitride liner 107 is formed.
[0034]
[Effect of the Invention] According to this invention, by removing the upper part of the silicon nitride liner of a trench intentionally, the electronic prehension by the silicon nitride liner of a trench and the hot carrier effect by this can be prevented, and the danger of a dent or a hump phenomenon can be controlled with a high accumulation component semiconductor device. Moreover, or it carries out a laminating in two steps, the gap philharmonic property of a trench may be raised with the combination of covering of the SOG film, and the laminating of other oxide films.
[0035] moreover -- silicon -- a nitride -- a liner -- a trench -- the upper part -- a field -- removing -- having -- alike -- following -- silicon -- a nitride -- a liner -- origin -- the purpose -- it is -- consecutiveness -- a process -- depending -- stress -- control -- it can decrease -- stress -- depending -- a trouble -- nothing -- the lower part -- a field -- **** -- a liner -- the advantage -- maintaining -- while -- the upper part -- the problem of an electron trap -- it can prevent .

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[Translation done.]

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## CLAIMS

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[Claim(s)]
[Claim 1] The phase which forms a trench etching pattern in a substrate and forms a trench by etching, The phase which forms a silicon nitride liner in the wall of a trench, and the phase which fills up said trench with the 1st reclamation oxide film, The phase of carrying out the recess of said 1st reclamation oxide film according to a wet process, and exposing the upper part of the liner of said trench, The formation approach of the trench component demarcation membrane of the semiconductor device characterized by including the phase where isotropic etching removes the upper part of said liner, and the phase which fills up with the 2nd reclamation oxide film the space where the recess of said trench was carried out.
[Claim 2] The phase which forms a trench etching pattern in said substrate is the formation approach of the trench component demarcation membrane of the semiconductor device according to claim 1 characterized by performing by carrying out the laminating of the silicon nitride to the substrate with which the pad oxide film was formed, and carrying out patterning to it.
[Claim 3] The formation approach of the trench component demarcation membrane of the semiconductor device according to claim 1 or 2 characterized by including the phase which forms the thermal oxidation film at the wall of said trench between the phase which forms said trench, and the phase which forms said liner.
[Claim 4] The formation approach of the trench component demarcation membrane of a semiconductor device given in any 1 term of claims 1-3 characterized by including the phase which carries out the laminating of the buffer oxide film on said liner between the phase which forms said liner, and the phase which fills up a trench with said 1st reclamation oxide film.
[Claim 5] The phase which carries out the recess of said 1st reclamation oxide film according to a wet process is the formation approach of the trench component demarcation membrane of a semiconductor device given in any 1 term of claims 1-4 characterized by carrying out until the front face of said reclamation oxide film becomes low below at the channel depth predetermined with said trench.
[Claim 6] The phase where isotropic etching removes the upper part of said liner is the formation approach of the trench component demarcation membrane of a semiconductor device given in any 1 term of claims 1-5 characterized by wet carrying out with a phosphoric-acid solution.
[Claim 7] Said trench is the formation approach of the trench component demarcation membrane of a semiconductor device given in any 1 term of claims 1-6 characterized by being limited to the trench of a P channel transistor field.
[Claim 8] The formation approach of the trench component demarcation membrane of a semiconductor device given in any 1 term of claims 1-7 characterized by including further the phase of carrying out CMP to said 2nd reclamation oxide film, and the phase of removing said trench etching pattern.
[Claim 9] Said 1st reclamation oxide film and said 2nd reclamation oxide film are the formation

approach of the trench component demarcation membrane of a semiconductor device given in any 1 term of claims 1-8 characterized by being formed by the CVD approach.
[Claim 10] It is the formation approach of the trench component demarcation membrane of a semiconductor device given in any 1 term of claims 1-9 characterized by forming at least one side by the SOG film among said 1st reclamation oxide films and said 2nd reclamation oxide films.
[Claim 11] The phase of removing the upper part of said liner is HDP. The formation approach of the trench component demarcation membrane of a semiconductor device given in any 1 term of claims 1-10 characterized by carrying out with the phase which fills up with said 2nd reclamation oxide film the space by which the recess was carried out by CVD.

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[Translation done.]